multiLane

DATASHEET

Innovation for the next generation

ML4039EN

4-Channel | 56 GBd PAM4 & NRZ | 400G BERT with ISI, JTOL & Crosstalk Noise injection|

4 x 56 GBd NRZ/PAM4 BERT | SSPRQ, PRBS13Q & PRBS31Q | 7-Tap PPG Linear Equalizers | Signal SNR, Histogram and Dynamic FFE | Programmable ISI Emulator to 9 dB | Shallow Loopback Testing | FEC

Summary

With the accelerated growth of hyperscale datacenters, the performance demands on Ethernet network infrastructure is increasing exponentially, and customer expectations for high-speed data throughput is at an all-time high. As a result, Bit Error Rate Testers (BERT) have become a cornerstone for physical layer testing, from qualifying bit transmission for fiber optic and copper-wire digital data transmission lines to testing signal integrity.

A BERT generates a sequence of bits through a communication channel and the received bits are then compared against the transmitted bits. A Bit Error Ratio (BER) evaluates the full end-to-end performance of a connectivity system and assures communication reliability.

The ML4039EN is a 4-channel, 56 GBd PAM4 & NRZ, 400G BERT with a unique crosstalk noise injection capability. It can be used in combination with ML407-PAM for jitter tolerance testing and has a programmable ISI emulator. Real hardware FEC testing is also possible with the versatile ML4039EN.

ML4039EN

4 x 56 GBd BERT

Introduction

The ML4039EN is a full feature 400G BERT that can be configured as a four-channel PAM4 56 GBaud or four-channel NRZ 28/56 Gbps lanes. Also, half rates of 23 to 29 GBd are supported.
The transmitters Support all standard test patterns mandated by IEEE and OIF such as PRBS13Q, SSPRQ, PRBS31Q, etc. It is also possible to program the TX to output a user-defined pattern.
The ML4039EN is specifically designed to add crosstalk noise with configurable frequency up to 29.6 Gbps for NRZ and up to 29.6 GBaud for PAM4. Additionally, the user can select to programmatically add an ISI channel equivalent to a frequency-dependent attenuator with 1 to 9 dB loss at Nyquist.
When used in conjunction with the ML407-PAM clock synthesizer, it can modulate its output pattern with SJ of over 5UI and up to 4 MHz.

Key Features

Transmit

- Data Rates: 23 – 29 & 46 – 58 GBd
- Ability to tune the bit rate in steps of 100 kbps and find the RX PLL locking margin
- Independent control of inner eye levels
- Up to 0.8 Vppd output swing
- Supports Gray coding and polarity inversion

Available patterns are:
  - PRBS7/9/11/13/15/16/23/31/58
  - PRBS13Q, PRBS31Q
  - SSPRQ
  - Square wave
  - Error injection
- 3-tap Pre- and Post-emphasis
- 7-tap linear TX FFE
- Programmable ISI Emulation

Receive

- SNR monitoring over time
- PAM4 histogram monitor
- PAM4 slicer threshold adaptive
- Error-detection on following patterns:
  - PRBS 7/9/11/15/16/23/31
  - PRBS13Q and PRBS31Q
- LOS indicators

General

- API libraries with documentation
- LabView sample and Python wrapper available
- Shallow Loopback testing
- Forward Error Correction (FEC)
  - Support generation of idle pattern with RS544/RS528 encoding types
  - Support FEC decoding on RX and FEC statistics measurement
- Crosstalk Injection
  - Configurable frequency in the range of 9-14.2 Gbps and 22-29.6 Gbps for NRZ and 22-29.6 GBaud for PAM4
- Same product available in ATE format for Advantest V93K

Target Applications

- Production testing of transceivers
- Functional and SI testing
- JTOL for 26 and 53 GBd receivers

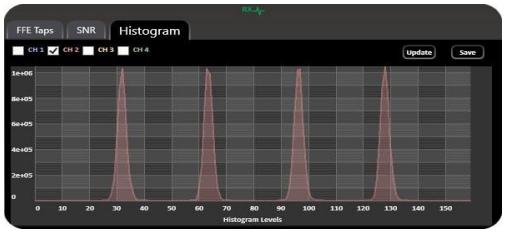

Figure 1: PAM4 eye histogram

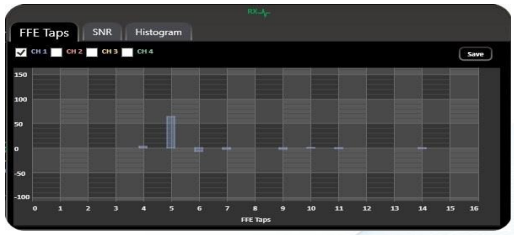

Figure 2: RX FFE Taps

Using ThunderBERT GUI both accumulated and instantaneous BER measurements can be monitored.

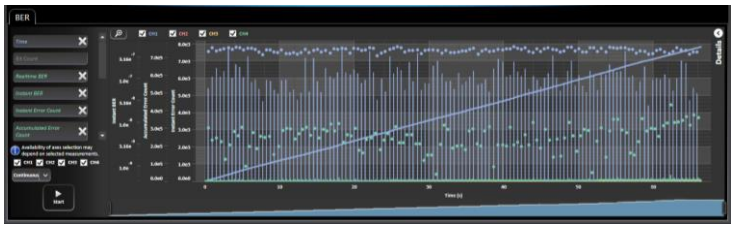

Figure 3: BER curves using ThunderBERT GUI

Block Diagram

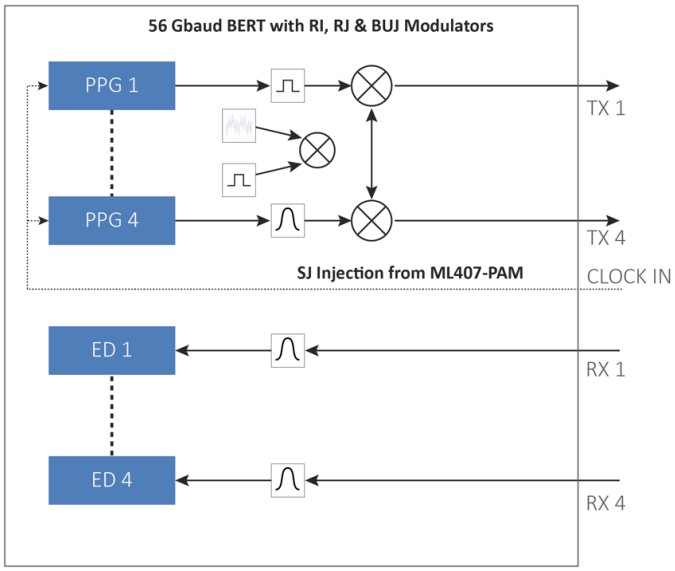

Figure 4: ML4039EN Block Diagram

SI Channel Emulation

The ML4039EN can programmatically emulate the effect of frequency-dependent attenuators with 1 dB up to 10 dB loss at the Nyquist frequency and a frequency roll-off similar to a PCB trace. When it comes to compliance testing on transceivers, more specifically for the stressed input test, this is highly practical. The effects of the different settings are shown in Fig. 5-10, both in eye diagram mode, as well as in pattern view.

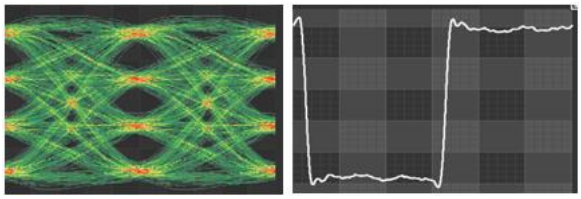

Figure 5: 1 dB ISI Channel

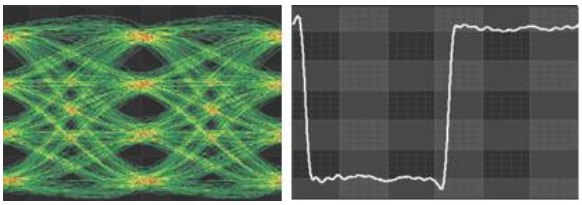

Figure 6: 2 dB ISI Channel

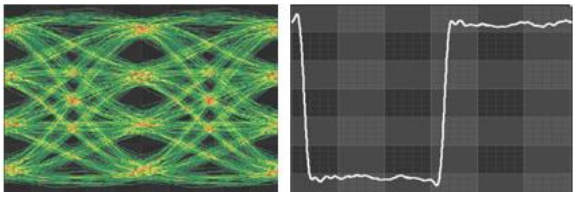

Figure 7: 3 dB ISI Channel

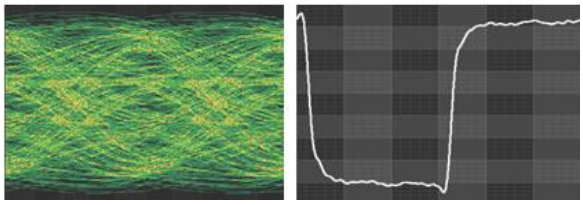

Figure 8: 4 dB ISI Channel

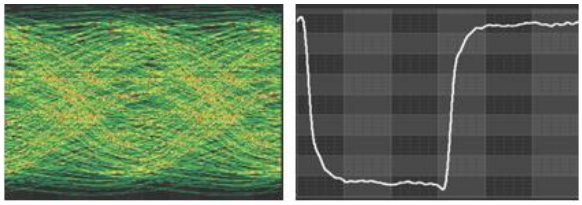

Figure 9: 5 dB ISI Channel

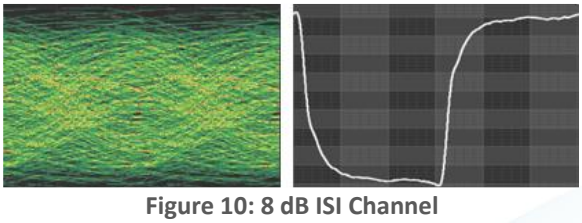

Figure 10: 8 dB ISI Channel

Jitter Tolerance Testing

The following measurement captures on 26/53 GBd PAM4 show the effects of crosstalk and jitter injection on a clean pattern.

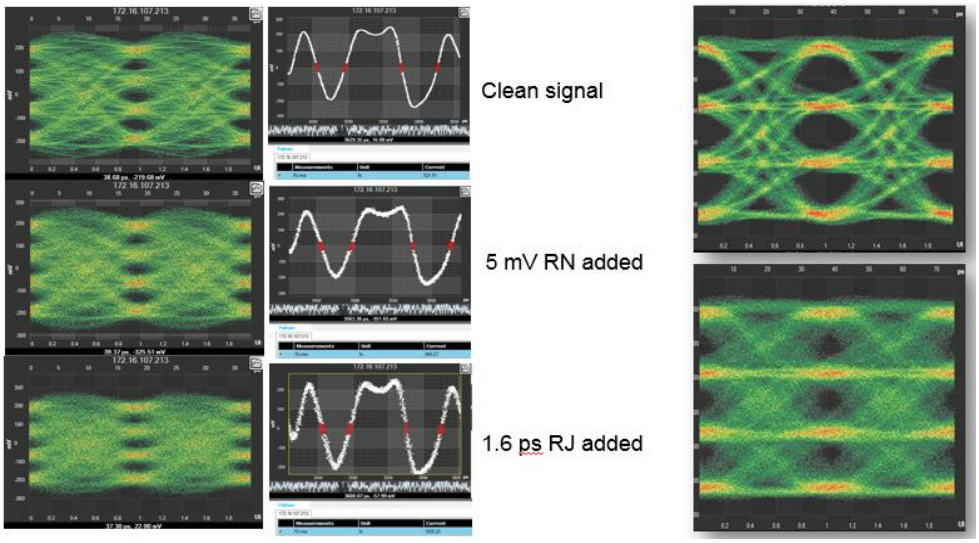

Figure 11: Adding impairments to a 26/53 GBd signal using the ML407-PAM clock synthesizer

Figure 12: JTOL Test Setup

Figure 13: ML407-PAM Clock Jitter Synthesizer

Noise Injection

The ML4039EN enables noise injection feature to emulate real-life crosstalk scenarios along with shallow loopback testing. Noise implementation can be done in the form of a continuous interference, burst crosstalk, or single shot noise and can be configured on each channel independently. The shallow loopback function works with a variety of traffic types including unframed PRBS, framed Ethernet and FEC traffic.

The following figure depicts a ML4039EN accepting traffic from an external 400G switch, looping the traffic back internally and re-transmitting it back to the RX side of the host.

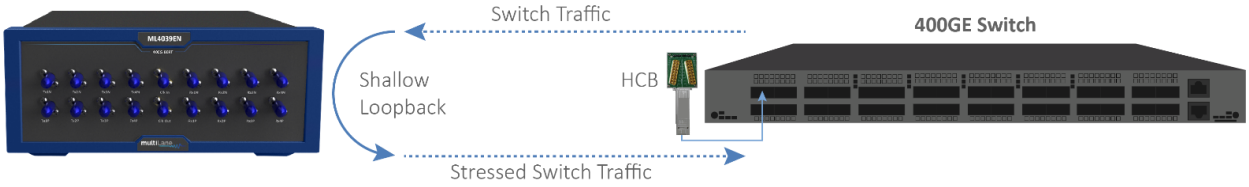

Figure 14: Shallow Loopback using ML4039EN and 400G switch

Electrical Specifications

Parameter		Specifications
Bit Rates		PAM4: 23 – 29 GBaud and 46 – 58 GBaud NRZ: 23 – 29 Gbps and 46 – 58 Gbps
TX Amplitude Differential		0 - 800 mVpp
Patterns		PRBS7/9/11/13/15/16/23/31/58 PRBS13Q, 31Q and SSPRQ Square wave & user-defined pattern
Linear Range		50 mV – 800 mV
TX Amplitude Adjustment		Steps of 2 mV
Pre- / Post-emphasis		6 dB
De-Emphasis Resolution		1000 steps
Equalizing Filter Spacing		1 UI
Random Jitter RMS		230 fs
Rise / Fall Time (20–80%)		12 ps / 14 ps
Coding		DFE Pre-coding and Gray coding supported
FEC (up to 400G stripes)		KP (100G, 400G) KR (100G)
Return Loss up to 10 GHz		< -18 dB
Return Loss (16-25 GHz)		< -15 dB
Error Detector input range		50 mV– 800 mV diff.
TX/RX connectors		2.4 mm connectors (2.92 mm optional)
Clock Output	**Reference clock**	Rate dividers 8/16/32/128
	Monitor Clock	156.25 MHz
Clock Input max		Up to 2.5 GHz
Clock Input Amplitude		750 mV single-ended
Input Impedance		50 Ω
Ambient Temperature		0-75 °C
Power		110 V, 1.4 A or 220 V, 0.9 A – 50/60 Hz

Mechanical Dimensions

The ML4039EN is a benchtop instrument that fits in a 19-inch 2U rack. Two ML4039ENs arranged side by side take up one 2U slot in your rack. MultiLane also supplies the needed brackets.

Ordering Information

Option	Description
ML4039EN	400G BERT (4 CH 56 GBd NRZ/PAM4)
3YW	Total 3-year warranty
CAL	Single calibration
3YWC	Total 3-year warranty with 3 annual calibrations
FEC	Real hardware FEC
29	2.92 mm connectors

Recommended Accessories

Instruments	Recommended *Phase matched cable pairs*	Alternative *Phase matched cable sets*	Comments
ML4039EN standard	8x MLCBPM-2.4-30	2x MLCBPM-2.4-30-8	2.4 mm connector 2x8 channel 30 cm
ML4039EN standard	8x MLCBPM-2.4-60	2x MLCBPM-2.4-60-8	2.4 mm connector 2x8 channel 60 cm
ML4039EN-29	8x MLCBPM-2.92-30	2x MLCBPM-2.92-30-8	2.92 mm connector 2x8 channel 30 cm
ML4039EN-29	8x MLCBPM-2.92-60	2x MLCBPM-2.92-60-8	2.92 mm connector 2x8 channel 60 cm

Please contact us at sales@multilaneinc.com.